

ABSTRACT

[0145] An ESD protection circuit for a semiconductor integrated circuit (IC) having protected circuitry, includes an SCR having at least one finger. Each finger includes a PNP transistor and an NPN transistor, where an emitter of the PNP and NPN transistors is respectively coupled between an I/O pad of the IC and ground, a base of the PNP transistor being coupled to a collector of the NPN transistor, and a base of the NPN transistor being coupled to a collector of the PNP transistor. The NPN transistor of each finger further includes a first gate for triggering said finger. A PMOS transistor includes a source and a drain respectively coupled to the I/O pad of the IC and the first gate of the NPN transistor. Further, a gate of the PMOS transistor is coupled to a supply voltage of the IC.